ABSTRACT

A data pipeline and clock control (relationship) that allows image data from a camera to pass directly through a display controller to an LCD without being written into, temporarily stored, and read out of a display buffer, e.g. a VRAM, is provided. Elimination of the video memory (VRAM) lowers the chip cost, reduces the power requirements, reduces delay due to writing and reading from the video memory, and reduces the pin count since fewer power pins are required.